SHEET INDEX

CONTENTS	SHEET NO.	SHEET ISSUE
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	6	2
CMS 144AJ	7	2
	8	2
	9	2
CMS 153A	10	2
	11	2

SYMBOL

DIAGNOSTIC ACCESS
ELEMENT A

TERM. MOD.	FUNCT	TERM.	LOC
BUFBDID	I	D13	3B1
CLRINIC	I	003	3BD
DRUTID	I	113	3B6
FCKID	I	207	2B2
FSIPCKID	I	104	2B2
INITID	I	307	2B2
IRMI1	I	218	3B5
IRPI1	I	318	3B6
IZMI1	I	316	3B5
IZPI1	I	317	3B5
SHSTPID	I	102	3B1
CLINIT1	#	D10	3B2
OIND	#	014	3B5
RRM1	#	213	3B7
RRP1	#	313	3B7
WZM1	#	214	3B7
WZP1	#	314	3B6
RESETO	#	506	3B1
SWFTO	#	109	3B5
+3	P	000,119,	2E7
GRD	G	200	
GRD	G	319	
SRD	G	060,260	2E7

ADDRESS & DATA
ELEMENT B

TERM. MOD.	FUNCT	TERM.	LOC
SAD17ID	I	005	2B3
AD17O	#	304	2E3
AD17A	#	210	
AD17B	#	311	
SADYTO	#	203	2E3

ERROR DETECTION
ELEMENT C

TERM. MOD.	FUNCT	TERM.	LOC
ERID	I	104	2B4
SERAID	I	206	2B4
TSERAD	#	205	2E4

REFRESH CONTROL
ELEMENT D

TERM. MOD.	FUNCT	TERM.	LOC
REFID	I	002	2B4

CONTROL AND TIMING
ELEMENT E

TERM. MOD.	FUNCT	TERM.	LOC
NLOID	I	105	2B5
PINITI1	I	004	2B3
SREQID	I	006	2B5
SREQO	#	302	2E5
PINITO	#	305	
TCKDA	#	201	
TCKDB	#	202	2E5

NOTES:

1. ⏚ GROUND RETURN
2. UNLESS OTHERWISE SPECIFIED:
   RESISTANCE VALUES ARE IN OHMS
   CAPACITANCE VALUES ARE IN MICROFARADS
   VALUES PRECEDED BY THE SYMBOL + (PLUS) OR − (MINUS) ARE IN VOLTS
3. BATTERY AND GROUND TERMINALS FOR INTEGRATED CIRCUITS

IC CODE	BAT. TERM.	GRD TERM.
144AJ	1,3B	19,2D
153A	14	1

4. BATTERY AND GROUND TERMINALS FOR THIS CIRCUIT PACK ARE AS FOLLOWS:

FUNCTION	TERMINAL
+3/	000,119
GRD	200,319,060,260

5. HORIZONTAL MOUNTING CENTER AT [illegible] INCHES.
6. CMS 153A IS CONTROLLED BY CPS FC200.

RECORD OF CHANGES

DWG ISS	PREV FURN	STD	MFR DISC	SEE NOTE

SYSTEM USED ON	DESIGN CONTROL
COMMON SYSTEMS	IH

MANUFACTURING REFERENCES

CATEGORY	NO.
CIRCUIT PACK CODE CONNECTOR ON FRAME	FC203
SERIES FOR CLASS "A" CHANGE. (ANY HIGHER SERIES IS ACCEPTABLE)	6

CURRENT DRAIN: 510mA

SHEET INDEX NOTES

1. WHEN CHANGES ARE MADE IN THIS DRAWING ONLY THOSE SHEETS AFFECTED WILL BE REISSUED.
2. THIS SHEET INDEX WILL BE REISSUED AND BROUGHT UP TO DATE EACH TIME ANY SHEET OF THE DRAWING IS REISSUED, OR A NEW SHEET IS ADDED.
3. THE ISSUE NUMBER ASSIGNED TO A CHANGED OR NEW SHEET WILL BE THE SAME ISSUE NUMBER AS THAT OF THE FIRST SHEET.
4. SHEETS THAT ARE NOT CHANGED WILL RETAIN THEIR EXISTING ISSUE NUMBER.
5. THE LAST ISSUE NUMBER OF THE FIRST SHEET INDEX IS RECOGNIZED AS THE LATEST ISSUE NUMBER OF THE DRAWING AS A WHOLE.

DWG ISSUE	ICE OR CD ISSUED	DATE ISSUE	DRAWN	APPD
1		12-28-76	MMS LRK	ACT LEG RFG
2A		1-8-76	DRM LRE	ACT LEG RFG

ISSUE 2A

1N98

FC203 CIRCUIT PACK

CLOCK CIRCUIT

AT&TCO STANDARD

(2)

CPS-FC203
11 SHEETS

BELL TELEPHONE LABORATORIES INCORPORATED

65

PART OF CPS FC203

CLOCK CIRCUIT

COMPONENT LIST

CAPACITOR

DESIG	CODE
[2] C1-C2	KS-20813 L4, 42.2PF
[5] C3-C7	KS-19774 L5, .01
C8	KS-19774 L1, 1200pF
C9	KS-20813 L4, 316pF
C10	KS-20813 L4, 215pF
[3] C11-C13	KS-19774 L4, .1

CRYSTAL

DESIG	CODE
Y1	1068B 14.9254

DIODE

DESIG	CODE
[3] CR1-CR3	458A
CR4	458C

INDUCTOR

DESIG	CODE
L1	KS-13726 L76, 4.22μH
L2	KS-13726 L24, 33μH

INTEGRATED CIRCUIT

DESIG	CODE
CM1	144AJ
CM2	153A

RESISTOR

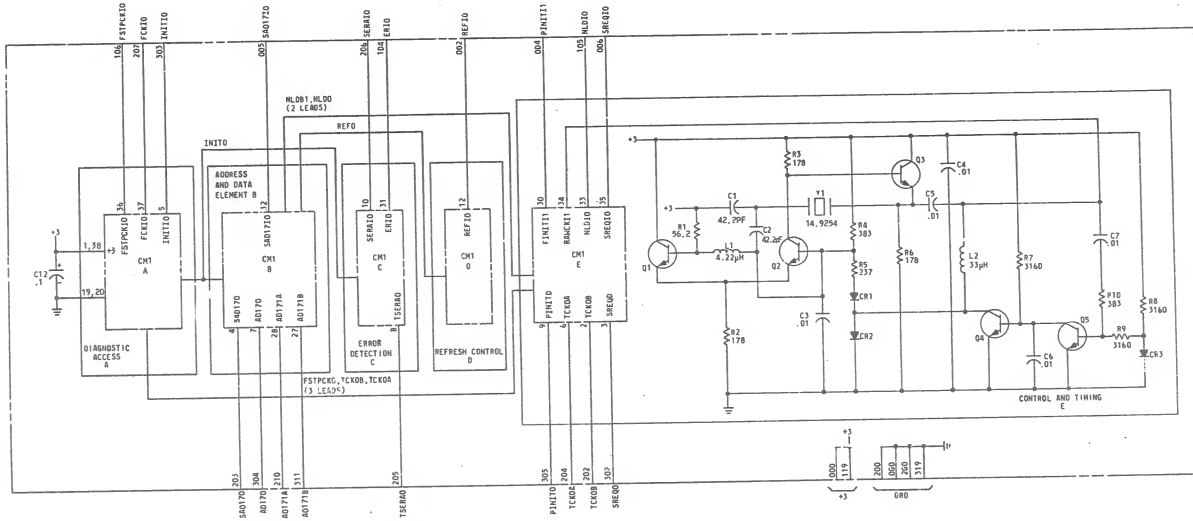
DESIG	CODE
R1	KS-20616 L1A, 56.2
[2] R2,R3	178
R4	383
R5	237
R6	178
[3] R7-R9	3160
R10	383
R11	511
R12	215D
R13	1210
R14	14.7
R15	2370
R16	237
R17	KS-20616 L1A, 2870

TRANSFORMER

DESIG	CODE
[4] T1-T4	2664G

TRANSISTOR

DESIG	CODE
[3] Q1-Q3	45A
[5] Q4-Q8	66J

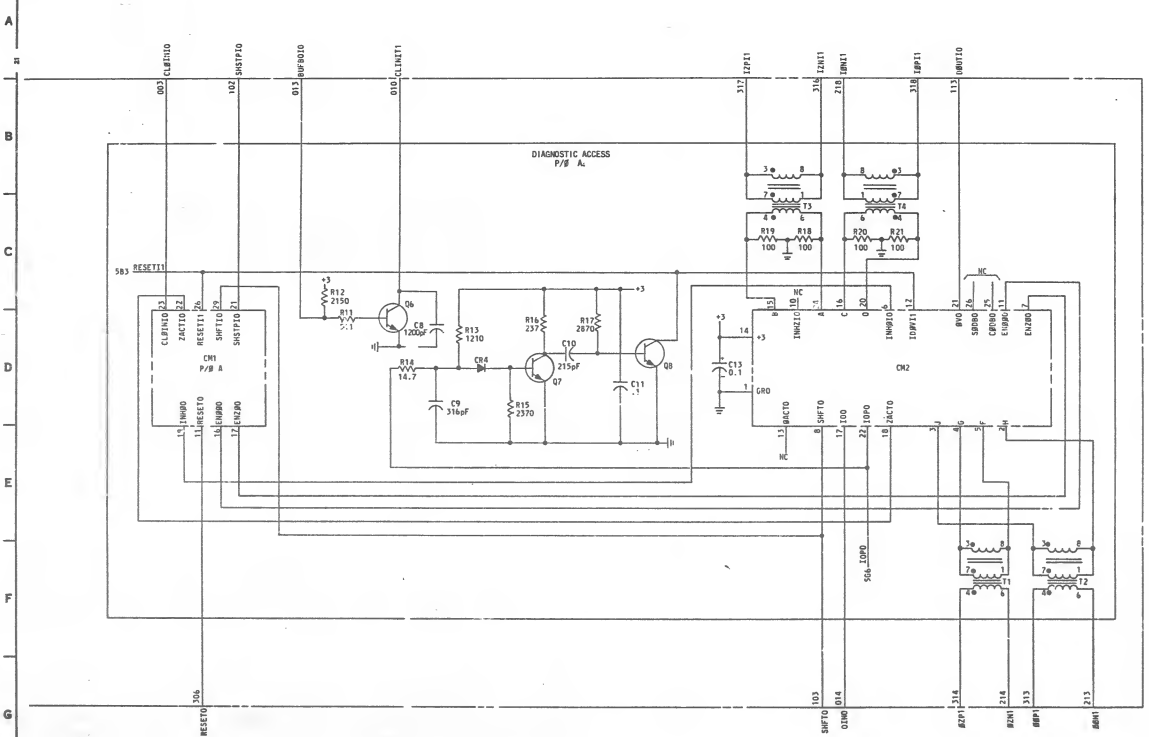


FC203 CIRCUIT PACK	2	CPS-FC203 SHEET 2
BELL TELEPHONE LABORATORIES INCORPORATED		6S

2A

PART OF CPS FC203

CLOCK CIRCUIT



FC203 CIRCUIT PACK	2	CPS-FC203 SHEET 3
BELL TELEPHONE LABORATORIES INCORPORATED	6S	

2A

PART OF CPS FC 203

CLOCK TIMING

CIRCUIT DESCRIPTION

A. FUNCTION

THE FC203 IS A CLOCK CIRCUIT PACK USED IN THE MAIN STORE CONTROLLER CIRCUIT (MASC). IT CONTAINS THE INTERFACE AND CONTROL CIRCUITS WHICH ENABLE COMMUNICATION WITH THE 3B CENTRAL CONTROL (3B CC) OVER THE SERIAL I/O CHANNEL (SIOC). IT ALSO CONTAINS THE MASC CLOCK OSCILLATOR AND ASSOCIATED CONTROLS, ONE BIT OF THE STORE ADDRESS REGISTER, AND AN ERROR REGISTER (ER) BIT.

B. DETAILED DESCRIPTION

NET NAME CONVENTIONS

A CONVENTION HAS BEEN CHOSEN AND USED FOR NET NAME MNEUMONICS:

1) THE LAST DIGIT OF A MNEUMONIC WILL BE EITHER 1 OR 0, INDICATING THE ACTIVE VOLTAGE LEVEL (HIGH OR LOW, RESPECTIVELY) OF THAT NET. E.G., NET SELIO IS ACTIVE WHEN VOLTAGE LOW.

2) IF THE LETTER IMMEDIATELY BEFORE THE LAST DIGIT IS AN I, THIS NET SERVES AS A SIGNAL INPUT TO THE CIRCUIT. E.G., SEL1O IS AN INPUT, WHILE SEL0 IS NOT.

3) IF THE LAST CHARACTER OF A NET NAME IS A LETTER, THIS NET IS A MEMBER OF A PARALLEL GROUP OF NETS CARRYING THE SAME SIGNAL. E.G., SELOA, SELOB, AND SELOC WOULD BE THREE PARALLEL NETS, CARRYING THE SAME INFORMATION.

4) IF THE LETTER IMMEDIATELY BEFORE THE LAST DIGIT IS A B, THIS NET SERVES AS A SERIAL DUPLICATION OF THE NET WITHOUT THE B. E.G. SELBO IS THE SERIAL DUPLICATE OF SEL0, SELBBO IS THE SERIAL DUPLICATE OF SELBBO, ETC.

5) THE OUTPUTS OF A HIGH-LEVEL REGISTER; I.E., A 2-BIT REGISTER OR GATED DELAY FLIP-FLOP, UNLESS OTHERWISE RENAMED, WILL BE ACTIVE IF THE REGISTER IS SET. E.G., IF NET ERR.Q1 IS THE Q1 OUTPUT OF REGISTER ERR, THEN ERR.Q1 WILL BE ACTIVE IF REGISTER ERR IS SET. IF THIS NET IS RENAMED ERRMPO, THE NET WILL BE ACTIVE ONLY IF REGISTER ERR IS CLEARED.

6) IF THE FIRST CHARACTER OF A NET NAME IS THE LETTER T, THIS NET WILL BE A COLLECTOR-TIE (OUTPUTS FROM TWO OR MORE GATES TIED TO THE SAME NET). E.G., TSELO IS SUCH A NET.

WHILE THESE CONVENTIONS HAVE BEEN CONSCIENTIOUSLY FOLLOWED, THERE WERE CIRCUMSTANCES THAT PRECLUDED THEIR USE. IN SUCH CASES, THE NET WILL BE SPECIALLY NOTED.

C. SYMBOL/LEAD MNEMONICS

MNEMONIC	DEFINITION
A0170	ADDRESS BIT 17 (OUTPUT)
A0171A	ADDRESS BIT 17 (OUTPUT TO BRANCH A)
A0171B	ADDRESS BIT 17 (OUTPUT TO BRANCH B)
BUFBOG	BUFFER BIT 0
CLINIT1	CLEAR INITIALIZE
CLRINIO	CLEAR THE CHANNEL ONE INHIBIT
OBUTIO	DATA OUT (TO SIOC FROM MASC)
ERIO	ERROR A REGISTER (INPUT)
FCKIO	FORCE CLOCK (DIAGNOSTIC INPUT)
FSTPCKIO	FORCE STOP CLOCK (DIAGNOSTIC INPUT)
GSA017O	ADDRESS BIT BIT 17 (OUTPUT TO HIGHER ORDER STORES)
GSREQO	STORE REQUEST (OUTPUT TO HIGHER STORES)
IOO	INPUT DATA (FROM SIOC TO MASC)
IKITIO	INITIALIZE
I0NI1	INPUT ONE, NEGATIVE (SIOC INPUT TO MASC NEGATIVE FROM CHANNEL ONE)
I0PI1	INPUT ONE, POSITIVE (SIOC INPUT TO MASC POSITIVE FROM CHANNEL ONE)
IZNI1	INPUT ZERO, NEGATIVE (SIOC INPUT TO MASC NEGATIVE FROM CHANNEL ZERO)
IZPI1	INPUT ZERO, POSITIVE (SIOC INPUT TO MASC POSITIVE FROM CHANNEL ZERO)
NLOIO	NORMAL LOAD
0ONI	OUTPUT ONE, NEGATIVE (SIOC OUTPUT FROM MASC NEGATIVE TO CHANNEL ONE)
0OPI	OUTPUT ONE, POSITIVE (SIOC OUTPUT FROM MASC POSITIVE TO CHANNEL ONE)
0ZNI	OUTPUT ZERO, NEGATIVE (SIOC OUTPUT FROM MASC NEGATIVE TO CHANNEL ZERO)
0ZPI	OUTPUT ZERO, POSITIVE (SIOC OUTPUT FROM MASC POSITIVE TO CHANNEL ZERO)
PINITIO	POWER INITIALIZE INPUT
PINITO	POWER INITIALIZE OUTPUT
REFIO	REFRESH
REFO	REFRESH MODE
RESETO	RESET OF I/O FUNCTIONS
SA017IO	ADDRESS BUS BIT 17 (INPUT)
SERAIO	STORE ERROR A (FROM HIGHER STORES)
SHFTIO	SHIFT
SHFTO	SHIFT (SIOC SHIFT SIGNAL)
SNSTPIO	SHIFT STOP
SREQIO	STORE REQUEST
TCKOA	CLOCK BRANCH A
TCKOB	CLOCK BRANCH B
TSERAO	STORE ERROR A OUTPUT

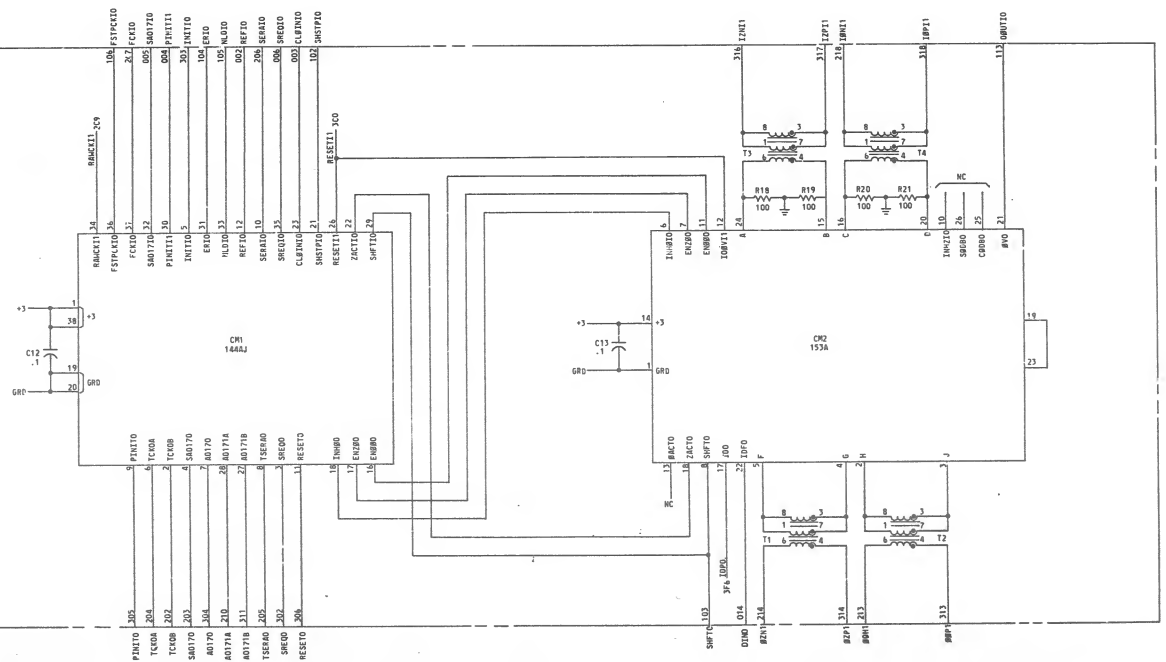
ISSUE 2A

FC203 CIRCUIT PACK (2) CPS-FC203 SHEET 4

BELL TELEPHONE LABORATORIES INCORPORATED 6S

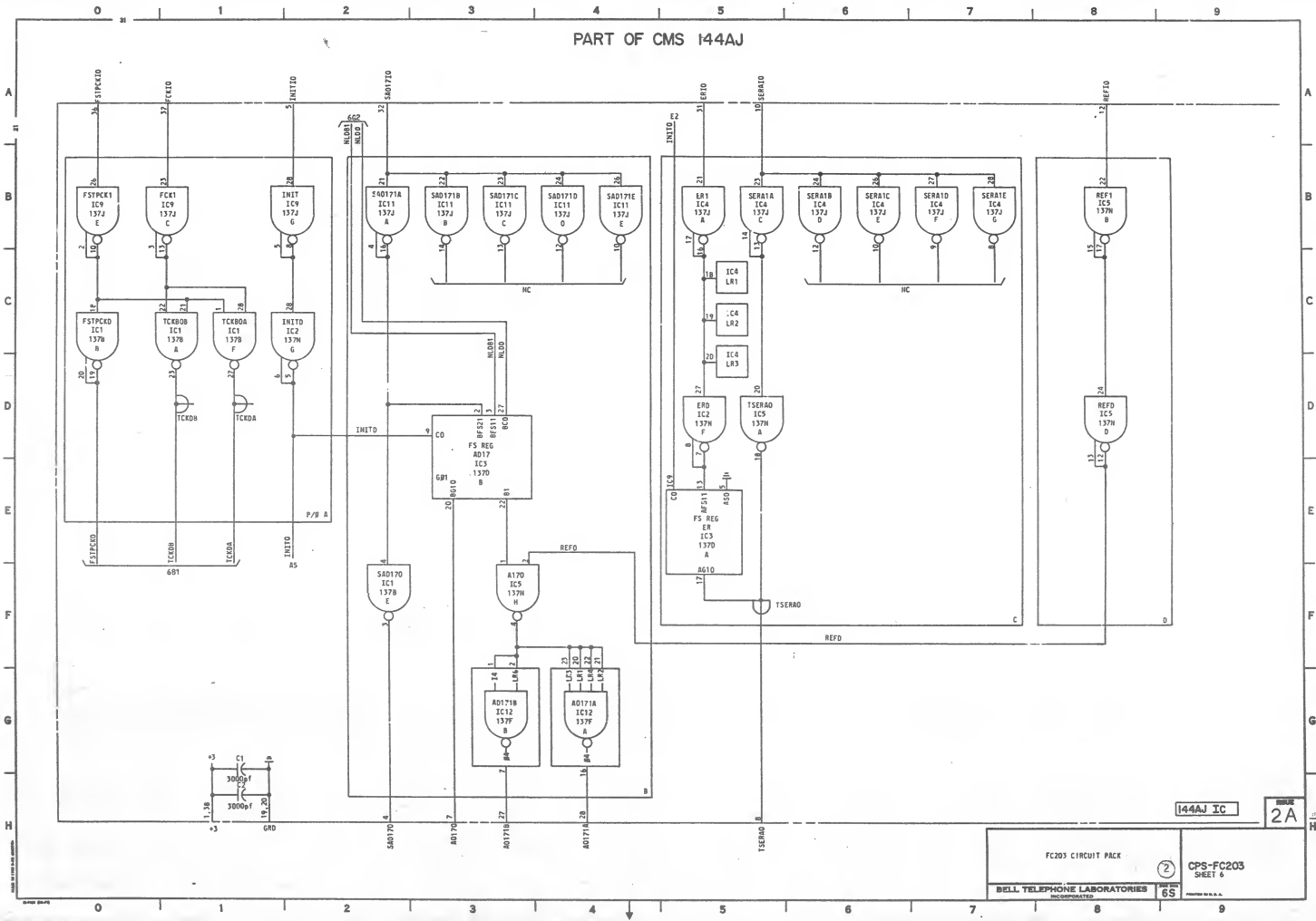
PART OF CPS FC 203

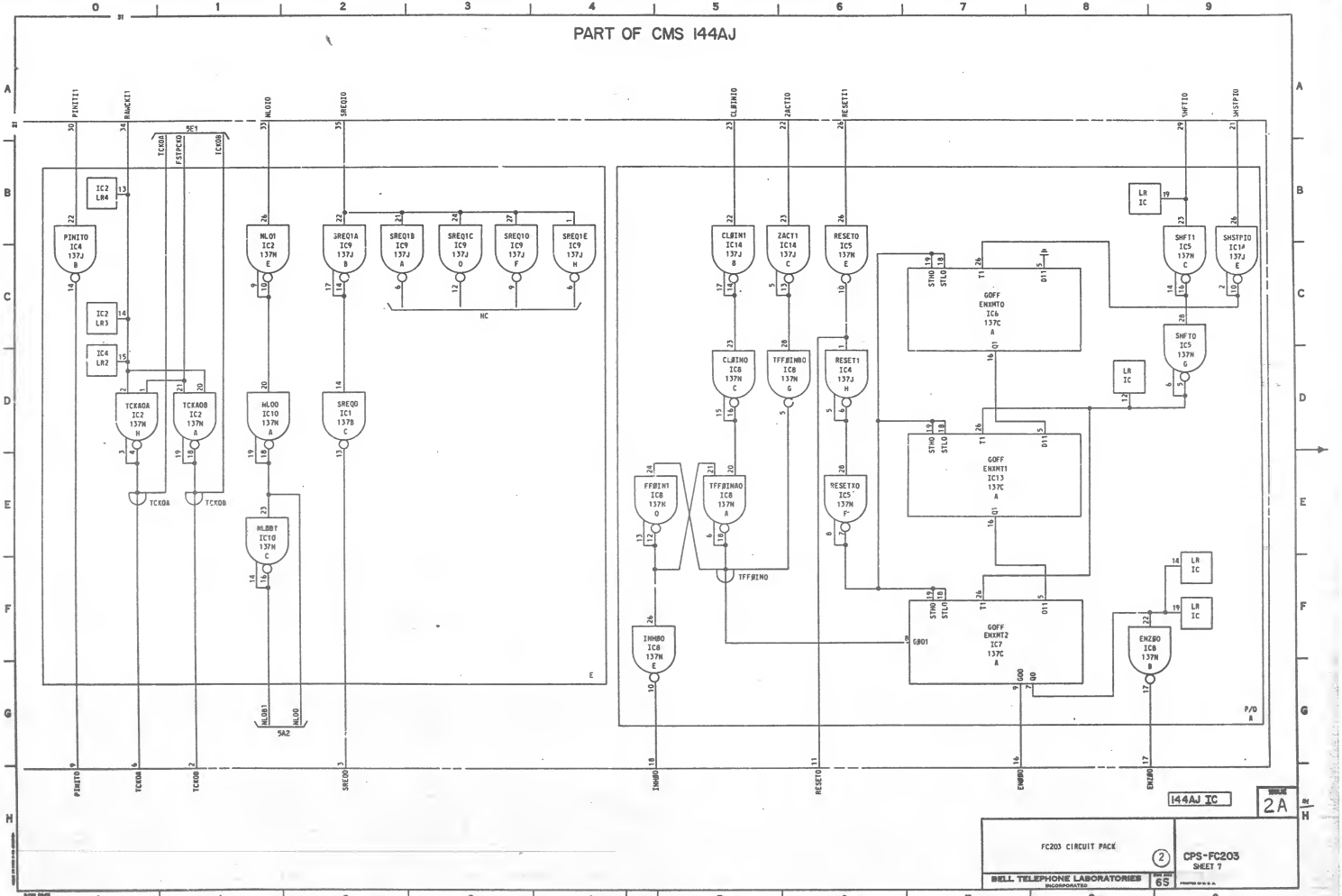
GENERAL BLOCK INTERCONNECTIONS



FC203 CIRCUIT PACK	CPS-FC203
BELL TELEPHONE LABORATORIES INCORPORATED	SHEET 5

2A


PART OF CMS 144AJ
FSTPCK1 IC9 137J E
FCK1 IC9 137J C
INIT IC9 137J G
FSTPCKO IC1 137B B
TCKB0B IC1 137B A
TCKB0A IC1 137B F
INITO IC2 137M G
P/S A
FSTPCKO
TCKDB
TCKDA
INITO
6B1
A5
SAD171A IC11 137J A
SAD171B IC11 137J B
SAD171C IC11 137J C
SAD171D IC11 137J D
SAD171E IC11 137J E
HC
NLOB1
NLOD
FS REG AD17 IC3 137D B
BFS21
BFS11
BCO
GB1
BO10
B1
INITO
REFO
SAD170 IC1 137B E
A170 IC5 137M H
AD171B IC12 137F B
AD171A IC12 137F A
+3
C1
3000pF
C2
3000pF
GND
E2
ER1 IC4 137J A
SERA1A IC4 137J C
SERA1B IC4 137J D
SERA1C IC4 137J E
SERA1D IC4 137J F
SERA1E IC4 137J G
IC4 LR1
IC4 LR2
IC4 LR3
ERD IC2 137M F
TSERAO IC5 137M A
FS REG ER IC3 137D A
AG10
REF1 IC9 137M B
REFD IC5 137M D
144AJ IC
2A
FC203 CIRCUIT PACK
CPS-FC203
SHEET 6
BELL TELEPHONE LABORATORIES
INCORPORATED
6S


PART OF CMS 144AJ
PINIT1
RAMCKT1
NL01D
SREQ1D
CLRINI0
ZACT1O
RESET1I
SHFT1O
SHSTP1O
PINIT1O
TCK0A
TCK0B
SRC0O
INH0O
RESET0
ENZ0O
144AJ IC
2A
FC203 CIRCUIT PACK
CPS-FC203
SHEET 7
BELL TELEPHONE LABORATORIES
INCORPORATED

PART OF CMS 144AJ

COMPONENT LIST

INTEGRATED CIRCUIT

LOC CODE ELEM ID	IC1 137B DESIG	SH LOC	IC2 137M DESIG	SH LOC	IC3 137D DESIG	SH LOC	IC4 137J DESIG	SH LOC	IC5 137M DESIG	SH LOC	IC6 137C DESIG	SH LOC	IC7 137C DESIG	SH LOC	LOC CODE ELEM ID
A	TCKBDB	5C1	TCKADB	6D1	ERAD17	5D3	ER1	5B5	TSERAD	5D5	ENXMTD	6F7	ENXMT2	6C7	A
B	FSTPCKD	5CD					PINITD	6BD	REF,	5B8					B
C	SREQC	6D2					SERA1A	5B5	SHFT1	6B9					C
D							SERA1B	5B6	REFD	5D8					D
E	SAD17D	5F2	HLD1	6B2			SERA1C	5B6	RESETD	6B6					E
F	TCKBDA	5C1	ERD	5D5			SERA1D	5B7	RESETXD	6E6					F
G			INITD	5C2			SERA1E	5B7	SHFTD	6C9					G
H			TCKADA	6DD			RESET1	6D6	A17D	5F3					H

LOC CODE ELEM ID	IC8 137N DESIG	SH LOC	IC9 137J DESIG	SH LOC	IC10 137H DESIG	SH LOC	IC11 137J DESIG	SH LOC	IC12 (NOTE 1) 137F DESIG	SH LOC	IC13 137C DESIG	SH LOC	IC14 137J DESIG	SH LOC	LOC CODE ELEM ID
A	TFFØINAD	6E5	SREQ1B	6B3	HLDD	6B1	SAD171A	5B2	AD171A	5G3	ENXMT1	6D7			A
B	EHZØD	6F8	SREQ1A	6B2			SAD171B	5B3	AD171B	5G3			CLØIN1	6B5	B
C	CLØINO	6D5	FCK1	5B1	HLDB1	6E2	SAD171C	5B3					2ACT1	6B6	C
D	FFEIN1	6E5	SREQ1C	6B3			SAD171D	5B4							D
E	INHØD	6F5	FSTPCK1	5BD			SAD171E	5B4					SHSTPIC	6B9	E
F			SREQ1D	6B4											F
G	TFFØINBD	6D6	INIT1	5B2											G
H			SREQ1E	6B4											H

CAPACITOR

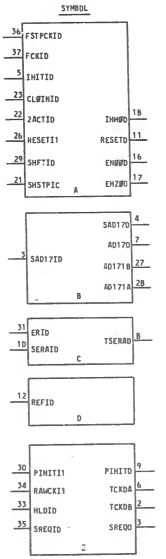
DESIG	CODE
[2] C1-C2	BD1A, 3000pf

NOTES:

1. A CAPACITOR CHIP (BD1A, 3000pf) IS BONDED ON EACH SIDE OF THE 137F SIC.

CIRCUIT DESCRIPTION

SYMBOL



BATTERY AND GROUND TERMINALS FOR THIS CIRCUIT MODULE

IC CODE	BAT TERM	GRD TERM
137B	25	11
137C	25	11
137D	25	11
137F	25	11
137J	25	11
137M	25	11
137N	25	11

SUPPORTING INFORMATION	
CATEGORY	NO.
INTEGRATED CIRCUIT CODE	144AJ
ONLY ACCEPTABLE SERIES	6

144AJ IC

ISSUE 2A

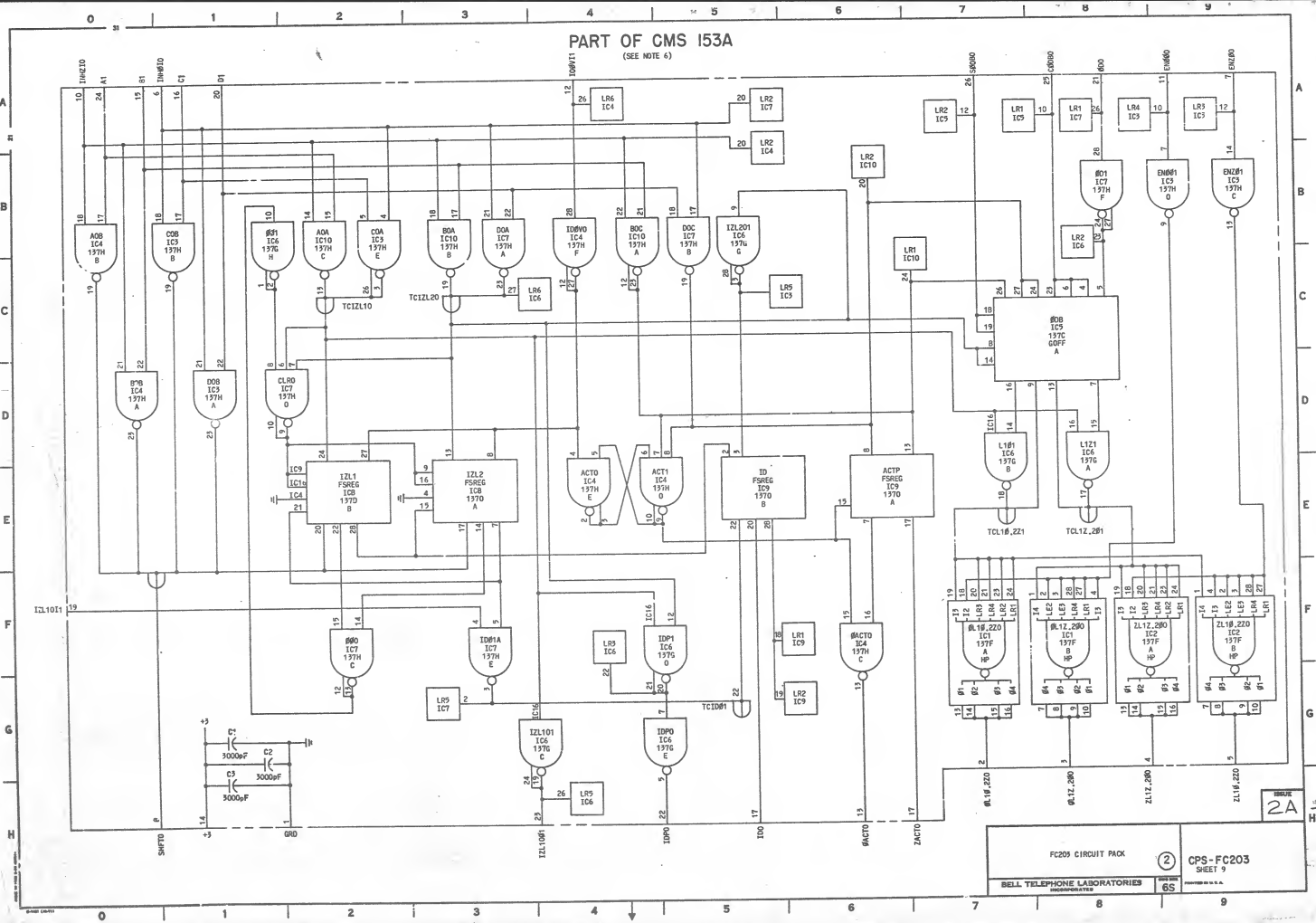
FC203 CIRCUIT PACK

(2)

CPS-FC203
SHEET 8

BELL TELEPHONE LABORATORIES INCORPORATED

65


PART OF CMS 153A
(SEE NOTE 6)
FC203 CIRCUIT PACK
2
CPS-FC203
SHEET 9
BELL TELEPHONE LABORATORIES
INCORPORATED
6S
ISSUE
2A

PART OF CMS 153A

(SEE NOTE 6)

COMPONENT LIST

INTEGRATED CIRCUIT

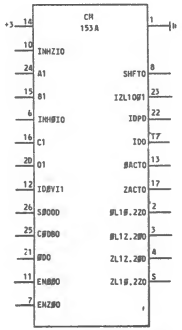
LOC CODE ELEM ID	IC1 137F (NOTE 1) DESIG	SH LOC	IC2 137F (NOTE 1) DESIG	SH LOC	IC3 137H OESIG	SH LOC	IC4 137H DESIG	SH LOC	IC5 137C DESIG	SH LOC	IC6 137G DESIG	SH LOC	IC7 137H DESIG	SH LOC	IC8 137D DESIF	SH LOC	IC9 137D DESIG	SH LOC	IC10 137H OESIG	SH LOC	LOC CODE ELEM ID
A	BL1B.22D	8F7	ZL1Z.28D	8F8	DOB	8D1	BOB	BDO	BDB	BCB	L1Z1	8E8	DOA	8B3	IZL2	8E3	ACTP	8E6	BOC	8B4	A
B	BL12.28D	CF8	ZL1B.22D	8F9	COB	8B1	ADB	B8O			L1B1	8G7	DOC	8B5	IZL1	8E2	ID	8E5	BDA	8B3	B
C					ENZB1	8B9	BACTD	BF6			IZL101	8G4	BBD	8F2					ADA	8B2	C
D					ENBB1	8B9	ACT1	BE4			IDP1	8F4	CLRD	8D1							D
E					CDA	8B2	ACTO	BE4			IDPO	8G5	IDBIA	8F3							E
F					BACTD	8F5	IDBVO	B84					BD1	8B8							F
G											IZL201	8B5									G
H											BD1	8B1									H

CAPACITOR

DESIG	CODE	
[3] C1-C3	BD1 A	3000 Pf

NOTES:
1. A CAPACITOR CHIP (BD1 A, 3000 Pf) IS BONDED ON EACH SIDE OF THE 137 F SIC.

SYMBOL



BATTERY AND GROUND TERMINALS FOR THIS CIRCUIT MODULE:

IC CODE	BAT TERM	GRD TERM
137C	25	11
137D	25	11
137F	25	11
137H	25	11
137H	25	11

SPECIAL MANUFACTURING REFERENCES

CATEGORY	NO.
CONTROLLING DRAWING	FC200
CIRCUIT PACK CODE	FC200

SUPPORTING INFORMATION

CATEGORY	NO.
INTEGRATED CIRCUIT CODE	153A
(ANY HIGHER SERIES IS ACCEPTABLE)	3-4

153A IC

2A

FC203 CIRCUIT PACK

BELL TELEPHONE LABORATORIES INCORPORATED

6S

CPS-FC203
SHEET 10

PART OF CMS 153A

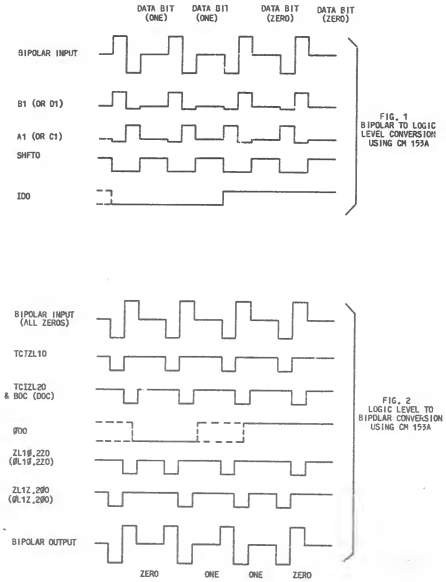


FIG. 1
BIPOLAR TO LOGIC LEVEL CONVERSION USING CM 153A

FIG. 2
LOGIC LEVEL TO BIPOLAR CONVERSION USING CM 153A

CIRCUIT DESCRIPTION

A. FUNCTION

CM 153A IS USED IN THE CONVERSION BETWEEN BIPOLAR SIGNALS ON THE 3A CC I/Ø DATA LINES AND LOGIC-LEVEL SIGNALS REQUIRED BY PERIPHERAL UNIT CONTROLLER CIRCUITS (SUCH AS THE TTY CONTROLLER).

B. DETAILED DESCRIPTION

LEADS HAVING DESIGNATIONS THAT END IN 1 ARE HIGH WHEN ACTIVE, OR IN THE ONE STATE. LEADS HAVING DESIGNATIONS THAT END IN Ø ARE LOW WHEN ACTIVE, OR IN THE ONE STATE. FLIP-FLOPS ARE SET TO THE ONE STATE AND CLEARED TO THE ZERO STATE.

BIPOLAR TO LOGIC LEVEL CONVERSION

THE CONTROLLER-RECEIVED DATA LINE IS TRANSFORMER-COUPLED TO CM 153A ON LEADS A1 AND B1 FROM CCO, AND C1 AND D1 FROM CC1. THE DATA IS ORED BY GATES ADA AND CDA AT TCIZL1Ø, AND BY GATES BDA AND DDN AT TCIZL2Ø. THE RELATIONSHIP BETWEEN THE BIPOLAR DATA, THE INPUT TO CM 153A, AND ITS LOGIC-LEVEL DATA (IDO) AND TIMING (SHFTO) OUTPUT SIGNALS, IS SHOWN IN FIG. 1. THE LOGIC STATE OF THE BIPOLAR DATA BIT IS DETERMINED BY THE ORDER OF ITS POSITIVE AND NEGATIVE EXCURSIONS. A LOGICAL ONE IS A POSITIVE LOBE FOLLOWED BY A NEGATIVE LOBE. A LOGICAL ZERO IS A NEGATIVE LOBE FOLLOWED BY A POSITIVE LOBE. CLIPPING CIRCUITS, WHICH ARE PART OF GATES TO WHICH THE A1, B1, C1, AND D1 INPUTS CONNECT, LIMIT THE NEGATIVE EXCURSION AT THIS POINT, AND PREVENT RECOVERY PROBLEMS IN THESE GATES.

THE INPUT DATA LEAD (IDO) IS SET AT THE LEADING EDGE OF THE FIRST LOBE. THE TIMING SIGNAL IS THE TRAILING EDGE OF SHFTO WHICH OCCURS AT THE TRAILING EDGE OF THE SECOND LOBE. THUS, THE CONTROLLER IS SIGNALED TO SAMPLE THE INCOMING DATA IN THE CENTER OF THE BIT PERIOD WHEN THE DATA LEAD IS STABLE. CARE HAS BEEN TAKEN TO MINIMIZE THE NUMBER OF GATES THAT CONTROL THE IDO AND SHFTO LEADS IN ORDER THAT VARIATIONS IN GATE DELAYS WILL NOT DESTROY THE RELATIONSHIP BETWEEN THESE SIGNALS. NOMINAL TIMES FOR THE 3A CC SERIAL I/Ø DATA ARE A 15Ø-NS BIT INTERVAL WITH 37.5-NS LOBES.

THE SHFTO LEAD IS CONTROLLED BY GATES ADB, BDB, CDB, AND DDB, AND FLIP-FLOPS IZL1 AND IZL2, INITIALLY, NONE OF THE GATES ARE ACTIVE AND BOTH FLIP-FLOPS ARE IN THE CLEARED STATE SO THAT SHFTO IS HIGH. IF IMH2ID AND IMHØID ARE NOT ACTIVE, THE FIRST LOBE OF THE INPUT DATA BIT WILL ACTIVATE ONE OF THE GATES (DEPENDING ON WHETHER THE BIT IS A ONE OR ZERO AND IF IT IS FROM CCO OR CC1) AND PULL SHFTO LOW. THE FIRST LOBE WILL ALSO ACTIVATE ONE OF THE GATES FORMING TCIZL1Ø OR TCIZL2Ø WHICH WILL SET ONE OF THE FLIP-FLOPS, IZL1 OR IZL2, DEPENDING ON CONDITIONS PREVIOUSLY DESCRIBED. THE PURPOSE OF THESE FLIP-FLOPS IS TO HOLD SHFTO LOW DURING ANY GAP THAT MIGHT BE PRESENT BETWEEN THE FIRST AND SECOND LOBES AND TO PREVENT THE SECOND LOBE FROM CHANGING THE STATE OF THE DATA FLIP-FLOP (IDO).

WHEN THE SECOND LOBE OF THE INCOMING DATA BIT IS ACTIVE THE MATE OF THE GATE ACTIVATED BY THE FIRST LOBE WILL BE ACTIVE, AND IT WILL ALSO HOLD SHFTO LOW (AOB AND BOB ARE MATES AS ARE COB AND DOB). THIS LOBE WILL ALSO SET THE FLIP-FLOP (IZL1 OR IZL2) THAT WAS NOT SET BY THE FIRST LOBE. WHEN THE SECOND FLIP-FLOP IS SET, IT INHIBITS THE PATH BY WHICH THE FIRST FLIP-FLOP HELD SHFTO TO GROUND. WHEN THE FIRST LOBE IS OVER ONLY THE GATE ACTIVATED BY THE SECOND LOBE HOLDS SHFTO LOW.

WITH BOTH FLIP-FLOPS SET, THE INPUT TO CLRO FROM ØØ1 IS HIGH. THE OTHER INPUTS TO CLRO, TCIZL1Ø, AND TCIZL2Ø ARE CONTROLLED BY THE DATA LOBES. WHEN THE FIRST LOBE IS DONE, ONLY THE SECOND LOBE CONTROLS CLRO. WHEN THE SECOND LOBE EXPIRES, THE GATE HOLDING SHFTO IS DISABLED AND SHFTO WILL GO HIGH. CLRO WILL GO LOW AT THIS TIME AND CLEAR BOTH FLIP-FLOPS. CLRO LOW ALSO BLOCKS THE IZL1 AND IZL2 CONNECTION TO SHFTO SO THAT FALSE SIGNALS CANNOT OCCUR ON THIS LEAD AS THE FLIP-FLOPS CHANGE FROM THE 11 TO THE ØØ STATE.

LEAD IDO IS CONTROLLED BY THE ID FLIP-FLOP. ID RETAINS THE LAST INCOMING DATA STATE UNTIL IT IS UPDATED BY THE FIRST LOBE OF A NEW DATA BIT. IF THE NEW DATA BIT IS A ZERO, TCIZL1Ø WILL BE ACTIVE FIRST AND DRIVE DATA IZL1Ø1 HIGH. TERMINALS 19 AND 23 ARE EXTERNALLY TIED TOGETHER SO THAT IDO1A HAS BOTH INPUTS HIGH. IT SHOULD BE NOTED THAT IZL1 AND IZL2 ARE INITIATED FROM THE CLEARED STATE AND THAT TCIZL1Ø SETS IZL1 BUT DOES NOT AFFECT IZL2. IDO1A WILL PULL TCIDØ1 LOW, WHICH WILL CLEAR ID AND DRIVE IDO HIGH, TO ITS ZERO STATE. WHEN THE SECOND LOBE IS ACTIVE FOR THE ZERO DATA BIT, TCIZL2Ø WILL DRIVE IZL2Ø1 HIGH. HOWEVER, IZL1 WAS SET BY THE FIRST LOBE, IN ORDER TO PREVENT IZL2Ø1 FROM CHANGING THE ID FLIP-FLOP.

IF THE INCOMING DATA BIT IS A ONE, TCIZL2Ø WILL BE ACTIVE FIRST, IZL2Ø1 WILL BE HIGH WHILE IZL1 IS CLEARED, AND THE ID FLIP-FLOP WILL BE SET. IDO WILL THUS BE LOW, WHICH IS THE ONE STATE. WHEN THE SECOND LOBE IS ACTIVE FOR AN INCOMING ONE, TCIZL1Ø IS ACTIVE, AND WILL DRIVE IZL1Ø1 HIGH. TCIZL2Ø, HOWEVER, WILL HAVE SET IZL2, WHICH PREVENTS IDØ1A FROM CHANGING ID.

LEADS ZACTO AND ØACTO INDICATE WHICH, IF ANY, CC IS ACTIVELY COMMUNICATING WITH THE CONTROLLER. THE ACT FLIP-FLOP, FORMED BY GATES ACTO AND AC11, IS SET BY GATES BOC ON DOC TO INDICATE THAT ONE OF THE CC'S IS SUPPLYING INPUT DATA. FLIP-FLOP ACTP IS SET BY BOC WHEN CCO IS ACTIVE, A 1S CLEARED BY DOC WHEN CC1 IS ACTIVE. THE ACT AND ACTP FLIP-FLOPS ARE COMBINED TO ACTIVATE ZACTO WHEN CCO IS ACTIVE AND ØACTO WHEN CC1 IS ACTIVE. BOTH THE ZACTO AND ØACTO ARE HIGH WHEN NEITHER CC IS ACTIVE.

IMH2ID AND IMHØID BLOCK INPUT DATA FROM CCO AND CC1 WHEN THEY ARE ACTIVE.

LEAD IDPO WILL BE ACTIVE WHEN EITHER LOBE OF THE INPUT DATA BIT IS PRESENT. IT CAN BE USED BY AN EXTERNAL CIRCUIT TO INDICATE WHEN INCOMING DATA IS PRESENT. THE EXTERNAL CIRCUIT MUST HAVE SUFFICIENT FILTERING TO HOLD OVER ANY GAP BETWEEN LOBES.

INPUT IDRVI IS USED TO INITIALIZE THE IZL1 AND IZL2 TO THE ØD STATE, AND TO CLEAR THE ACT FLIP-FLOP. THIS SIGNAL MAY BE ACTIVATED BY AN EXTERNAL CIRCUIT AT THE END OF A DATA COMMUNICATION.

LOGIC LEVEL TO BIPOLAR CONVERSION

THE 3A CC FOLLOWS THE DATA PORTION OF A COMMUNICATION TO A PERIPHERAL UNIT WITH AN ALL-ZEROS BIT STREAM. THIS BIT STREAM IS USED BY THE PERIPHERAL UNIT AS BIT TIMING FOR THE BIPOLAR DATA SENT TO THE 3A CC. THE 3A CC MAINTAINS THE ALL-ZEROS BIT STREAM UNTIL IT RECEIVES A REPLY FROM THE PERIPHERAL UNIT, OR UNTIL THE MAXIMUM INTERVAL IN WHICH IT SHOULD RECEIVE A REPLY IS EXCEEDED. THUS, FOR EACH OUTGOING BIT PERIOD, LEAD A1 IS ACTIVE FOLLOWED BY B1 ACTIVE. INPUTS ENZØO AND ENØOO ARE ACTIVATED TO START THE OUTPUT AND DIRECT IT TO CCO OR CC1.

GATES ZL1Ø,2ZO AND ZL12,28O ARE TRANSFORMER-COUPLED TO THE OUTGOING DATA LINE TO CCO. GATES ØL1Ø,2ZO AND ØL12,28O ARE TRANSFORMER-COUPLED TO THE OUTGOING DATA LINE TO CC1. THESE GATES ARE HELD HIGH WHEN THERE IS NO INCOMING DATA OR WHEN THE ENABLE LEAD (ENZØO, ENØOO) IS NOT ACTIVE.

THE RELATIONSHIP BETWEEN THE ALL-ZEROS INPUT DATA, THE LOGIC LEVEL OUTGOING DATA LEAD, AND THE BIPOLAR OUTPUT DATA IS SHOWN IN FIG. 2. THE LOGIC LEVEL OUTGOING DATA SIGNAL (ØDO) IS TOGGLED INTO ØDB PRIOR TO THE BIT PERIOD. THE OUTPUT OF ODB IS COMBINED WITH THE TIMING SIGNALS DERIVED FROM THE INCOMING DATA (TCIZL1Ø AND TCIZL2Ø) TO DETERMINE THE ORDER IN WHICH TCL1Ø,2Z1 AND TCL12,28I WILL BE ACTIVE. IF A ONE IS TO BE SENT, TCL1Ø,2Z1 WILL BE ACTIVE DURING THE FIRST LOBE AND TCL12,28I WILL BE ACTIVE DURING THE SECOND LOBE. THE REVERSE WILL BE TRUE TO OUTPUT A ZERO. THESE SIGNALS WILL BE INVERTED BY THE ENABLED OUTPUT GATES ZL1Ø,2ZO AND ZL12,28O AND/OR ØL1Ø,2ZO AND ØL12,28O.

A GATE IN EACH PAIR IS CONNECTED TO THE OPPOSITE END OF THE PRIMARY OF A TRANSFORMER; EACH PAIR OF GATES IS PROVIDED WITH A TRANSFORMER. THUS, THE ORDER IN WHICH THE GATES ARE ACTIVE DETERMINES THE POLARITY OF THE PULSE AVAILABLE AT THE TRANSFORMER SECONDARY WINDING. NOTE THAT THE STATE OF THE ØDO LEAD IS TOGGLED INTO ØDB BY BOC (OR DOC) DURING THE BIT INTERVAL PRECEDING THAT IN WHICH THE BIT IS TRANSMITTED. INPUTS SØDBO AND CØDBO ALLOW DIRECT SET AND CLEAR OPERATIONS ON ØDB.

SYMBOL/LEAD

C. MNEMONICS

MNEMONIC	DEFINITION
ACTP	SET OR CLEARED TO DETERMINE WHICH INPUT PORT IS ACTIVE
ACTO,1	SET WHEN EITHER INPUT PORT IS ACTIVE
A1,B1	INPUTS FROM CCO
CØDBO	CLEAR ODB FF
C1,D1	INPUTS FROM CC1
ENØØO	ENABLE OUTPUT TO CC1
ENZØO	ENABLE OUTPUT TO CCO
ID	INCOMING DATA
IDMVI1	INCOMING DATA OVER, INPUT
IDPO	INCOMING DATA PRESENT
IZL1	INCOMING ZERO LOBE ONE - SET BY FIRST LOBE WHEN INPUT IS ZERO
IZL2	INCOMING ZERO LOBE TWO - SET BY SECOND LOBE WHEN INPUT IS ZERO
IDO	INCOMING DATA
ØACTO	CC1 IS ACTIVE
ØDB	OUTGOING DATA
ØDO	OUTGOING DATA BIT
ØL1Ø,2ZO	FIRST LOBE FOR A ONE, SECOND LOBE FOR A ZERO TO CC1
ØL12,28O	FIRST LOBE FOR A ZERO, SECOND LOBE FOR A ONE TO CC1
SHFTO	SHIFT
SØDBO	SET ODB FF
ZACTO	CCO IS ACTIVE
ZL1Ø,2ZO	FIRST LOBE FOR A ONE, SECOND LOBE FOR A ZERO TO CCO
ZL12,28O	FIRST LOBE FOR A ZERO, SECOND LOBE FOR A ONE TO CCO

ISSUE 2A

FC2Ø3 CIRCUIT PACK (2)

CPS - FC2Ø3
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